ISSN: 2277-9655
(I2OR), Publication Impact Factor: 3.785

IJESRT

INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY

SDRAM CONTROLLER DESIGN FOR DATA ACQUISITION ON XILINX SPARTAN 3E FPGA

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ABSTRACT

In the modern electronics equipments that uses the memory, efficient and High speed memory controllers are must. Memory controllers will control the data flow in all electronic equipments such as Mobile Phones, Computers, Audio Video devices etc. Large number of signals can be sent or received at a time to the memory device. But sending or receiving the data directly will cause more traffic which degrades the performance of the device. In order to overcome such issues the memory controller is designed. User cannot directly interface with the memory device. In this project we are designing a memory controller the acts as an interface to control the signals efficiently between the SDRAM and user. A SDRAM memory device is used in order to decrease the latency and power consumption. The user interface can be done using the USB device. Design of this memory controller was done by considering many constraints. Designed memory controller uses the Xilinx platform which configured with DDR2 as the FPGA component.

KEYWORDS: Key DDR2**,** FPGA**,** Memory, SDRAM, USB.

INTRODUCTION

In the present generation of the memory devices high speed is the most important requirement that needs to be considered. The memory controller design had let a lot of designers to design more number of electronic components with less risk. However the design of device using the clock is always a risk factor. Design of the memory controller has considered many challenges such as memory support, device support, I/O support.

Memory controller eases the data transfer between the user and the memory device. In multiport devices memory controller will help to select the desired port. It allows the user to connect various types of devices that use the same Input/ Outputs. The most important feature of memory controller is memory sharing. Static memory controllers are mostly used where the data transfer rate is predictable. In these types of design the controller output is always predicted. The scheduling is done at the time of designing the controller. Dynamic memory controllers are used where the flexibility of the design is preferred. In dynamic memory controller the refresh command will always be activated where there is a no interface for a large amount of time. Here it is very difficult to calculate the memory efficiency. [1]

SDRAM (Synchronous Dynamic Random Access Memory) is also a DRAM which uses the clock pulses for responding to the user inputs. The first generation of SDRAMs was SDR (Single Data Rate) Based on the latency and performance the SDRAM have further generations as DDR (Double data rate), DDR2, DDR3 and DDR4 SDRAMs. The main difference between SDR and DDR was the bandwidth which was more available in DDR. [2]

In the present days use of SDRAM chips devices has increased in most of the electronics. Earlier only DRAMs and SRAMs were popular. As SRAMs consumed less power and were inexpensive, SRAMs were preferred most in the earlier days in cell phones, digital cameras. The memory requirement was increased as the era of new electronic devices emerged. Even though the SRAMs were cheaper, but had the small volume storage. Cascading of large number of SRAMs turned out to be very expensive. In order to increase the efficiency and storage volume in the electronics devices use of DRAMs started. For different type of applications we need different type of memory requirements. As the memory requirements go high there will be increase in cost as well. It is therefore required to develop a chip that will be reliable and cheap.

LITERATURE SURVEY

Qiu Daqiang, Hu Bing, Li Dandan (2007) described in their paper "Design of SDRAM Controller in High-Speed Data Acquisition Based on PCI Bus" that used PCI bus as the communication interface between the user and SDRAM device. The controller design was compose of the FIFO module, PCI bus, address module and the data module. The design was modeled to work at 5MHz and 40 MHz for refresh module.
The memory controller designed by these authors did not just increase the memory space but also was made to operate accurately and effectively. Two FSMs were designed one was for the initialization and the other FSM was for the main block of the SDRAM controller.
The controller was designed such a way that it could solve the connection problem through PCI bus. The module was designed using the verilog code. The design also concluded that the memory related issue in the earlier SRAM was resolved using the SDRAM. [3]
Referring this paper made us to understand the properties of SDRAM accessed in page mode and burst mode.

In 2011 Dechun Jung, Yang Yang and Ying Zhang of China published a paper with the title "FPGA realization of multi-port SDRAM controller in real time image acquisition system". The paper explained mainly the basic parts of SDRAM controller and how the multiport SDRAM can be implemented.
Multi-port controller was designed using FPGA for acquisition of real time images. The image was sent to the device in form of packets or bits based on the communication interface. Large volume of data was send to device using the communication interface (Either serial or parallel port). The communication interface was chosen based on the Volume, speed of the image that is to be processed.
This paper helped us to understand about how the SDRAM can be used as multiple virtual ports and access it. Different applications can be developed by using different FIFO techniques. [4]
In 2008 Sven Heithecker and Rolf Ernst of Institute of Computer and Communication Network Engineering Technical University of Braunschweig publish a paper that was helpful in controlling the traffic for FPGAs in complex application applications. In this paper they explained the importance of usage of SDRAM in complex devices. Optimization of SDRAM access is commonly a difficult task. Therefore a Controller is designed in order to access the SDRAM conveniently and effectively. To handle the complexity a two stage scheduling algorithm is developed. The main application of this paper was SDRAM used in video based applications.
Improving memory throughput will increase the memory latency. This is because of buffering needed to access the high end applications. Memory latency can be controlled using various arbitration techniques. This paper explained the technique to handle two types of QoS requirements. One is the smallest possible latency and the other one is the maximum throughput.
In 2010 Soo Yun Hwang, Dong Soo Kang, Hyeong Jun Park, and Kyoung Son Jhang proposed in their paper named "Implementation of a Self-Motivated Arbitration Scheme for the Multilayer AHB Busmatrix" explains the working of arbitration in multilayer advanced high-performance bus. The arbiter was designed to perform the arbitration between master and slave side. Arbitration in master side is different from slave side. A flexible arbiter was implemented for multilayer bus matrix. The design was made using priority basis such as round robin, dynamic priority and fixed priority. The design was also designed using three multiplexing modes, transfer, transaction and desired transfer length. Self motivation was the main scheme proposed to design the arbiter. Proposed design consists of input stage, command stage and output stage. Input stage was used to hold address and control information when transfer between the master and slave is not yet started. Command stage is used to send the signals to the desired slave location and output stage is used to show the experimental results and send the acknowledgements back to the master stage.

PROPOSED DESIGN

The project is implemented using the FPGA board. The signals are given by the user through user interface. The communicating device provides the handshake signals which control the system by providing the control, address and data signals.

General Architecture of Proposed Design

The block diagram for proposed design is shown in the figure below
The block contains of the USB interface that accepts the signals from user. The control signals given by the user are sent to the FPGA. All the memory operations that are read/write are handled by FPGA. Appropriate signals are further read or written to the memory device (SDRAM).
The USB interface is able to communicate with the memory controller. The memory controller board is configured with the USB port, through which the signals are sent to the USB port of the communicating device. The controller module performs all the sequences of signals needed for reading, writing, refreshing the memory module. The device selector will generate the appropriate signals to activate memory controller.

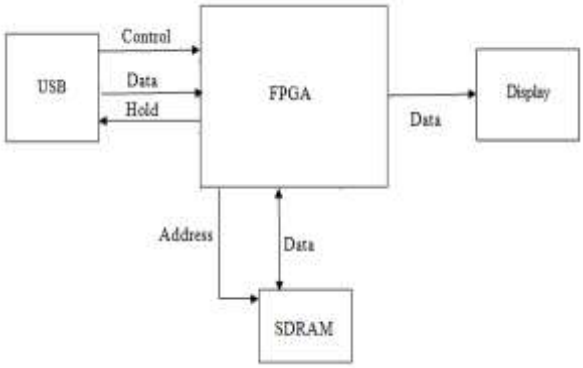

Fig-1: General Block Diagram Of memory Controller

The device is programmed for USB interface since we cannot connect the FPGA device directly to USB. USB along with some library functions allows user to interface with the components present in the board. The signals generated by the USB program are designed in such a way that all the signals are compatible with Spartan 3E FPGA device. Designed memory controller performs the following functions.

Standard signals are generated for communication through USB.

Appropriate signals generated are given to the FPGA device to establish communication. Generate the address, data and control signals separately. Read or write operation are carried according to the requirement

Generated the wait signal whenever there is the process of reading and writing is going on. Sometimes read or write will be carried without waiting for the processor to complete

Generation of wait signal will be dependent on the data register. The FPGA device is responsible to declare read or write operations. Address assigning is also done by the FPGA device.

Address by the USB can be assigned either to the Read register or the Write Register. Assigning of the address can be sometimes coupled with Read as well as write. The unique address should be assigned to each of the registers for both USB and FPGA device.

The FPGA interaction is required to ensure that the connection is properly made to the USB. Once the connection is set up the FPGA component decides which type of transfer method is used to transfer the data. It may use the wait signal or can communicate without using the wait signal. The clock period of about 20ns will be given once the output pin of USB port is activated. If the USB output signal is inactive then there is the no connection made. If active the launch process of the register takes place and hence transfers the necessary signals.

At the beginning of collection of data, the necessary parameter is sampling frequency. And trigger condition, appropriately given by host. Once the triggering condition is completed the data transfer to the memory device takes place. The data conversion will take place once the trigger condition satisfies. The data sent will be compared with the data module and will be sent to the refresh module if any refreshing of the circuit is required. Refreshing is done every 64 ns after the refreshing is done the data will be sent to the client device where it reads or write to the processer as per the trigger condition required. These are the steps for the data collection and once data collection is done the data will be read in page mode. [5]

The memory controller decodes the address into rows banks and columns. The data converted will be sent to and from the memory using banks. A clock module is use to distribute clock signal to al the modules connected. The acknowledgement bus is given back to the processor component. At the memory device the data is tested and received. If the data is valid an acknowledgement is sent to the processor saying that the data received is valid. Else there will be other acknowledgement message sent saying invalid data received. A data up to 16 MHz can be sent to the memory device. [6]

Tools Used

In design and implementation of the project following tools (Hardware and software) tools were used

1. Spartan 3E project kit.
2. Xilinx ISE (14.4) design suite for VHDL coding of the design.
3. ISim Simulator for analyzing the simulation results.
4. Xilinx Plan Ahead Software for assigning the pins of Xilinx

Power Supply Usage
Power supply for the device is about 1.7 to 1.95 V for the core device operation.
I/O power supply required by the multiplexers and buffers is 1.7 to 3.6 V.

ADVANTAGES

1) Low power consumptions.
2) Provision of mobility due to USB interface used.
3) Replaces earlier arbiters.
4) High transfer rate due to presence of on chip memory.
5) Easy to access.
6) Due to its property of general programmable interface it has replaced most of the parallel interface devices.
7) Low cost of SDRAMs.

APPLICATIONS

a) Used in most of the mobile phones
b) Due to its frequency of operation it is used in most of the real time devices.
c) Large, fast memory devices are required in networking and communications applications, with tasks ranging from simple address lookups to traffic shaping/policing to buffer management.
d) SDRAMs improve memory bandwidth by eliminating wait states or idle cycles between read and write cycles.
e) In wireless applications, low power memory is important, especially for handset and mobile devices, while high-performance is important for base station applications.

RESULTS

The results for proposed memory controller are given below

Initial State

During this state the signals given are

- Reset signal is kept 0
- Address bus is given as 1
- Data bus is initialised to 0

Fig-2: Initialisation Process

Write data with active wait

During this state the signals given are

- Reset signal is kept 1
- Address bus is given as 1
- Data bus is initialised to 0
- Write enable is 1

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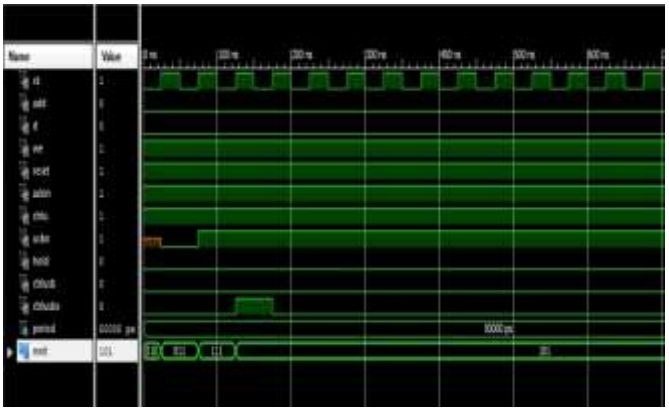
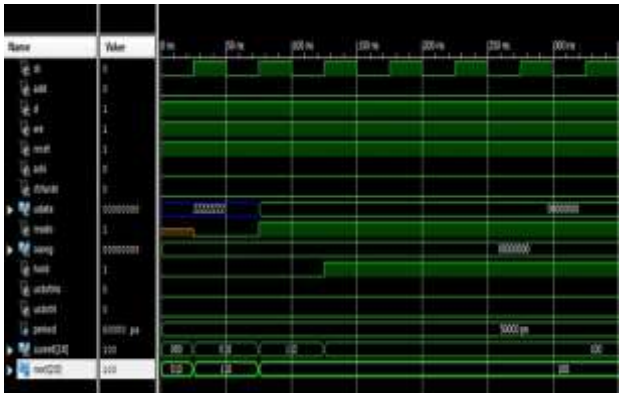


Fig-3: Write process with valid data

Read data with active wait

During this state the signals given are

- Reset signal is kept 1
- Address bus is given as 0
- Data bus is initialised to 1
- Write enable is 0
- Hold signal is 1



CONCLUSION

The paper demonstrates the design of the memory controller and its applications in general. The possible modifications to the basic edition of the device are proposed which can be less power consuming than previous version. Hence, it can be observed that SDRAM can be used as further improvements in design.

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ISSN: 2277-9655
(I2OR), Publication Impact Factor: 3.785

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